

Attorney Docket No. 10559-270001 Serial No.: 09/675,816 Amendment dated November 10, 2003 Reply to Office Action dated September 9, 2003

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

(Currently amended) A method of handling instructions
 within a processor comprising:

decoding at least a portion of an instruction eoded in a first code to determine a first destination and a second destination of the instruction;

re-encoding the at least only a portion of the instruction to a second re-encoded code if necessary used for said first destination and; and forwarding the re-encoded instruction to [[a]] said first destination; and

forwarding a different portion of the instruction, without re-encoding, to said second destination.

- (Canceled)
- 3. (Currently amended) The method of Claim [[2]] 1, further comprising sending at least a portion of the coded instruction to wherein said first destination is a first functional unit which operates based on op codes.

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- 4. (Currently amended) The method of Claim [[2]] 3, further comprising sending at least a portion of the decoded instruction to a second functional unit which operates based on decoded information.
- 5. (Original) The method of Claim 1, further comprising determining a portion of the coded instruction to decode.
 - (Canceled)
- 7. (Original) The method of Claim 1, further comprising handling instructions in a digital signal processor.
- 8. (Currently amended) A method of processing instructions within a processor comprising:

receiving [[an]] a coded processor instruction which is coded in a first code;

determining at least a destination location for a first functional unit which operates based on coded instructions, a second functional unit which operates based on decoded information obtained from the coded instruction, and a third functional unit, which each receive parts of the instruction;



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forwarding any a first portion of the coded instruction having a first destination location of a representing the first functional unit, to the first location functional unit;

decoding any remaining another portion of the instruction;

forwarding any said another portion of the decoded

instruction having a second destination location of the second location

representing the second functional unit, to the second location

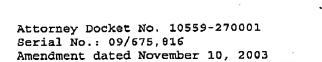
functional unit;

re-encoding any remaining portion of the instruction to a second code if necessary; and

forwarding the re-encoded instruction to a third location representing the third functional unit.

9. (Canceled)

10. (Currently amended) The method of Claim [[9]] 8, further comprising forwarding any portion of the decoded instruction having a destination location of a second location to wherein said second functional unit is a data address generator.



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- 11. (Currently amended) The method of Claim [[9]] 8, further comprising forwarding the re-encoded instruction to wherein the third functional unit is a system pipe.
- 12. (Original) The method of Claim 8, further comprising processing instructions within a digital signal processor.
- 13. (Original) The method of Claim 8, further comprising decoding and re-encoding with a decoder.
 - 14. (Currently amended) A processor comprising:

a decoder which receives an instruction coded in a first code and decodes at least a portion of the instruction to determine a first destination and a second destination of the instruction and forwards a portion of the instruction to said first destination, which operates based on a decoded code;

an encoder which re-encodes the at least a portion of the instruction to a second encoded code used for said second destination.

15. (Original) The processor of Claim 14, wherein the decoder determines the destination of the instruction.

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- 16. (Original) The processor of Claim 15, wherein the decoder forwards control signals to other portions of the processor.
- 17. (Original) The processor of Claim 16, wherein the control signals may be in the first code or the second code.
- 18. (Original) The processor of Claim 14, wherein the processor is a digital signal processor.